REMARKS

Figure 8C was included with filing of the Patent Application, as indicated in the specification. However, the figure corresponding to Figure 8C was originally mislabeled as Figure 8B. Please find attached the amended figures in which Figures 8, 8A and 8B, have been re-labeled as Figures 8A, 8B and 8C, consistent with the specification.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM Corporation Deposit Account No.09-0447. No extension of time is believed to be necessary. However, in the event an extension of time is required, that extension of time is hereby requested. Please charge any fee associated with an extension of time to IBM Corporation Deposit Account No.09-0447.

Respectfully submitted,

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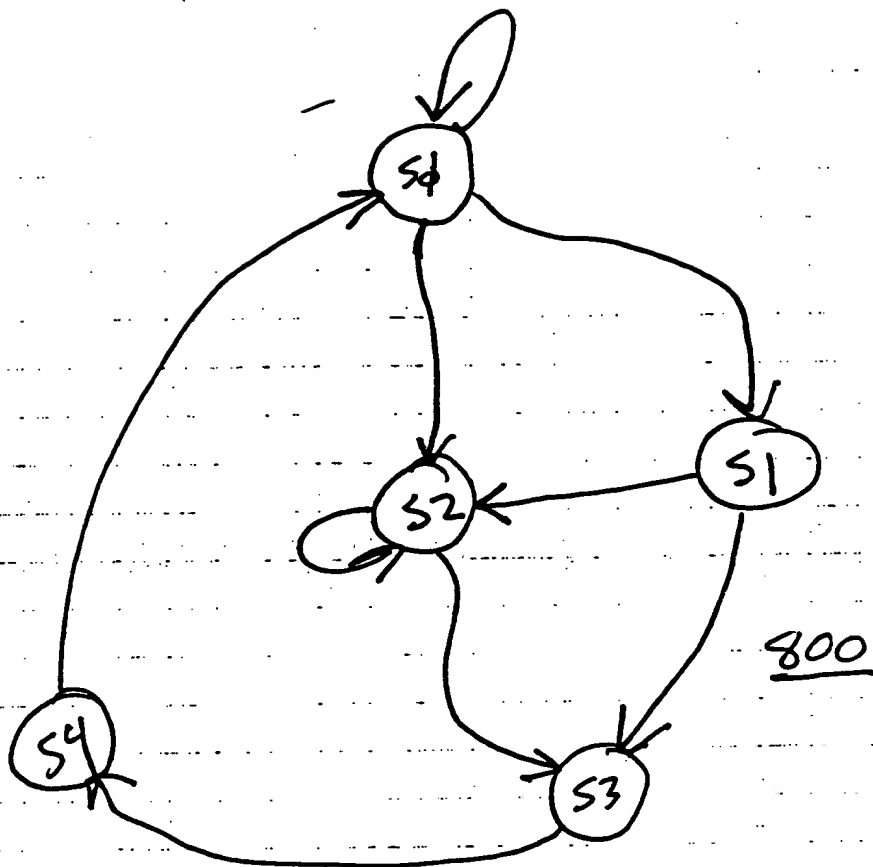(512) 343-6116

ATTORNEY FOR APPLICANT(S)

800

FIG. 8A (Amended)
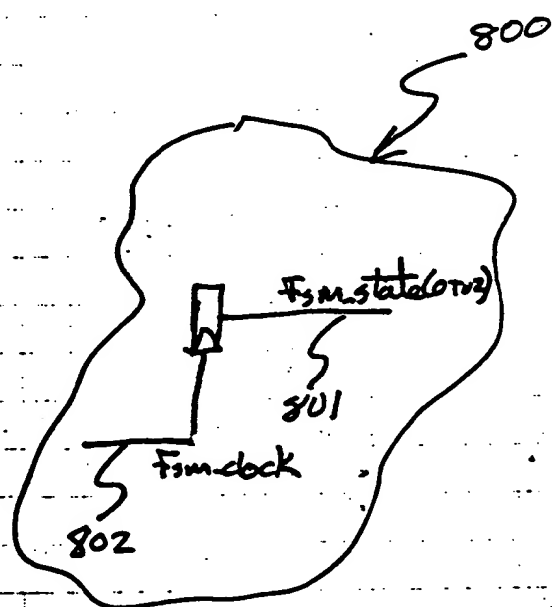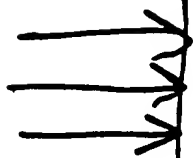
(Prior Art)

entity Fsm: Fsm

850

800

Fsm_state(0TV2)

801

Fsm_clock

802

FIG. 8B (Amended)
(Prior Art)

```
entity Fsm Is
  PORT(
        .... ports for entity Fsm.....
     );

  ARCHITECTURE Fsm of Fsm Is

  BEGIN

        .... HDL code For Fsm and rest of the entity...

        Fsm_state(0 to 2) <= ... signal 801....
853 {   --!! Embedded Fsm : exampleFsm;
859 {   --!! clock        : (Fsm_clock);
854 {   --!! state_vector : (Fsm_state(0 to 2));
855 {   --!! states       : (s0,s1,s2,s3,s4);
856 {   --!! state_encoding : ('000', '001', '000', '011', '100');
857 {   --!! arcs         : (s0=>s0, s0=>s1, s0=>s2,
        --!!                  s1=>s2, s1=>s3, s2=>s2,
        --!!                  s2=>s3, s3=>s4, s4=>s0);
858 { --!! end Fsm;
```

852

8C

                 END;

                 FIG. 8C (Amended)